UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,516	04/16/2004	Husam N. Alshareef	TI 37691	1947

23494 7590 02/21/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EV

Office Action Summary	Application No.	Applicant(s)	
	10/826,516	ALSHAREEF ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004 and 09 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *12-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 23-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-16-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 16 April 2004 and to applicant's election received on 09 December 2005.

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-11, 23-33 in the reply received on 09 December 2005 is acknowledged.

Claims 12-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 5-6, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilk et al. (US 6,291,282 B1).

Referring to Figs. 3d-3e and column 4, line 4 to column 5, line 49, Wilk et al. disclose a method of forming CMOS devices with metal gates that includes the following features:

- A metal gate electrode (326) that can be tantalum, molybdenum, or titanium is formed over a silicon substrate (301) as shown in Fig. 3d;
- The metal gate electrode (326) is patterned to form gate electrodes corresponding to a PMOS device (302) and to an NMOS device (304) as shown in Fig. 3e;

- The gate electrode corresponding to the NMOS device (304) is masked (328) (i.e. is protected by a mask layer) while the unmasked gate electrode (327) corresponding to the PMOS device (302) undergoes a nitridation treatment to change its work function as shown in Fig. 3e;
- The nitridation treatment preferably occurs by incorporating nitrogen gas in a plasma; and
- An additional layer of conductive material that can be tungsten can subsequently be included with the gate electrodes (326, 327) as described in column 5, lines 44-49.

These are all of the limitations set forth in claims 1-2, 5-6, 11 of the applicant's invention.

5. Claims 1-6, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hu (US 2002/0195679 A1).

Referring to Figs. 2-4 and paragraphs [0025] to [0033], Hu discloses a method of forming CMOS devices with metal gates that includes the following features:

- A metal silicide interconnecting layer (106) that can include tantalum or tungsten is deposited over a semiconductive silicon substrate (104) as shown in Fig. 2;
- A photoresist layer (110) (i.e. a protective layer) is applied to selectively mask PMOS regions (112) as shown in Fig. 2;

- The metal silicide interconnecting layer (106) corresponding to the unmasked NMOS regions (14) is then nitrided by plasma annealing in order to reduce its work function as shown in Fig. 2;
- The photoresist layer (110) is then stripped and a conductive layer (124) of low resistivity material that can be tungsten (i.e. a cladding layer) is then deposited on the interconnecting layers (106, 120) as shown in Fig. 3; and
- The conductive layer (124) and interconnect layers (106, 120) are then patterned into plural gate stacks (126) as shown in Fig. 4.

These are all of the limitations set forth in claims 1-6, 11 of the applicant's invention.

6. Claims 1-4, 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Rotondaro et al. (US 2003/0062577 A1).

Referring to Figs. 1A-1E and paragraphs [0014] to [0030], Rotondaro et al. disclose a method of forming CMOS transistors with metal gates that includes the following features:

- A metal layer (40) is deposited over a silicon substrate (20) as shown in Fig. 1A;
- A silicon germanium layer (50) for adjusting the work function of metal layer (40) is deposited over the metal layer (40) as shown in Fig. 1A;
- The silicon germanium layer (50) can be deposited by a plasma enhanced chemical vapor deposition method;
- The silicon-germanium layer is then patterned as shown in Fig. 1B;

- The patterned silicon-germanium layer is then annealed to form a silicon-germanium metal layer (70) with the corresponding adjusted work function as shown in Fig. 1D;
- The silicon-germanium metal layer (70) and the remaining metal layer (40) are then patterned to form gate electrodes 90, 92, respectively, with different work functions as shown in Fig. 1E; and
- An optional cladding layer (100) to reduce sheet resistance that can be tungsten or titanium nitride can be formed over the silicon-germanium metal layer (70) and the remaining metal layer (40) before patterning to form gate electrodes (90, 92) as shown in Fig. 1E and as described in paragraph [0029].

These are all of the limitations set forth in claims 1-4, 9-10 of the applicant's invention.

7. Claims 1-2, 6-8, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Chau et al. (US 6,890,807 B2).

Referring to Figs. 3a-3d and column 5, line 6 to column 7, line 10, Chau et al. disclose a method of forming CMOS devices with metal gates that includes the following features:

- A metal layer (202) that can be molybdenum, tungsten, tantalum, or ruthenium (also see column 3, lines 9-28) is formed over a semiconductor substrate (200) (also see column 2, lines 17-30) as shown in Fig. 3a;

- Portions of the metal layer (202) corresponding to NMOS devices are masked with photoresist (216) (i.e. a protective layer) while the unmasked portions corresponding to PMOS devices are doped to increase the work function of the metal as shown in Fig. 3c;
- Dopants used to increase work function can include oxygen, which can be deposited using plasma deposition methods (also see column 4, lines 15-18, 34-38); and
- The metal layer (202) is then patterned to form gate electrodes (220, 230) corresponding to an NMOS device and to a PMOS device (220) as shown in Fig. 3d.

These are all of the limitations set forth in claims 1-2, 6-8, 11 of the applicant's invention.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 23-25, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilk et al. (US 6,291,282 B1) in view of Zhu et al. (US 6,133,079).

Referring to Figs. 3d-3e and column 4, line 4 to column 5, line 49, Wilk et al. disclose a method of forming CMOS devices with metal gates that includes the following features:

- A metal gate electrode (326) that can be tantalum, molybdenum, or titanium is formed over a silicon substrate (301) as shown in Fig. 3d;
- The metal gate electrode (326) is patterned to form gate electrodes corresponding to a PMOS device (302) and to an NMOS device (304) (i.e. field effect transistors) as shown in Fig. 3e;
- The gate electrode corresponding to the NMOS device (304) is masked (328) (i.e. is protected by a mask layer) while the unmasked gate electrode (327) corresponding to the PMOS device (302) undergoes a nitridation treatment to change its work function as shown in Fig. 3e;
- The nitridation treatment preferably occurs by incorporating nitrogen gas in a plasma; and
- An additional layer of conductive material that can be tungsten can subsequently be included with the gate electrodes (326, 327) as described in column 5, lines 44-49.

These are limitations set forth in claims 23-25, 31 of the applicant's invention.

However, Wilk et al. do not expressly teach or suggest forming interconnects within dielectric layers located over the transistors to form an operational circuit, which are limitations of independent claim 23.

Referring to Fig. 4 and column 4, lines 33-61, Zhu et al. teach a method of forming a CMOS structure that includes forming inter level dielectric (ILD) (52) and inter metal dielectric (IMD) (55, 58) layers over field effect transistors (42, 44). The ILD and IMD layers include metal levels (54, 57, 59) that are interconnected using conductive vias (53, 56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Wilk et al. and Zhu et al. in order to include the formation of overlying dielectric layers with interconnections, as taught by Zhu et al. Zhu et al. recognize that a multi-level metallization network is used in integrated circuits for wiring discrete semiconductor devices (e.g. field effect transistors) together to thereby create desired circuits (see column 1, lines 14-19).

10. Claims 23-25, 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu (US 2002/0195679 A1) in view of Zhu et al. (US 6,133,079).

Referring to Figs. 2-4 and paragraphs [0025] to [0033], Hu discloses a method of forming CMOS devices with metal gates that includes the following features:

- A metal silicide interconnecting layer (106) that can include tantalum or tungsten is deposited over a semiconductive silicon substrate (104) as shown in Fig. 2;
- A photoresist layer (110) (i.e. a protective layer) is applied to selectively mask PMOS regions (112) as shown in Fig. 2;

- The metal silicide interconnecting layer (106) corresponding to the unmasked NMOS regions (14) is then nitrided by plasma annealing in order to reduce its work function as shown in Fig. 2;
- The photoresist layer (110) is then stripped and a conductive layer (124) of low resistivity material that can be tungsten (i.e. a cladding layer) is then deposited on the interconnecting layers (106, 120) as shown in Fig. 3; and
- The conductive layer (124) and interconnect layers (106, 120) are then patterned into plural gate stacks (126) as shown in Fig. 4.

These are limitations set forth in claims 23-25, 31-33 of the applicant's invention.

However, Hu does not expressly teach or suggest forming interconnects within dielectric layers located over the transistors to form an operational circuit, which are limitations of independent claim 23.

Referring to Fig. 4 and column 4, lines 33-61, Zhu et al. teach a method of forming a CMOS structure that includes forming inter level dielectric (ILD) (52) and inter metal dielectric (IMD) (55, 58) layers over field effect transistors (42, 44). The ILD and IMD layers include metal levels (54, 57, 59) that are interconnected using conductive vias (53, 56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Hu and Zhu et al. in order to include the formation of overlying dielectric layers with interconnections, as taught by Zhu et al. Zhu et al. recognize that a multi-level metallization network is used in

integrated circuits for wiring discrete semiconductor devices (e.g. field effect transistors) together to thereby create desired circuits (see column 1, lines 14-19).

11. Claims 23, 28-30, 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotondaro et al. (US 2003/0062577 A1) in view of Zhu et al. (US 6,133,079).

Referring to Figs. 1A-1E and paragraphs [0014] to [0030], Rotondaro et al. disclose a method of forming CMOS transistors with metal gates that includes the following features:

- A metal layer (40) that can be cobalt is deposited over a silicon substrate (20) as shown in Fig. 1A;
- A silicon germanium layer (50) for adjusting the work function of metal layer (40) is deposited over the metal layer (40) as shown in Fig. 1A;
- The silicon germanium layer (50) can be deposited by a plasma enhanced chemical vapor deposition method;
- The silicon-germanium layer is then patterned as shown in Fig. 1B;
- The patterned silicon-germanium layer is then annealed to form a silicon-germanium metal layer (70) with the corresponding adjusted work function as shown in Fig. 1D;
- The silicon-germanium metal layer (70) and the remaining metal layer (40) are then patterned to form gate electrodes 90, 92, respectively, with different work functions as shown in Fig. 1E; and

- An optional cladding layer (100) to reduce sheet resistance that can be tungsten or titanium nitride can be formed over the silicon-germanium metal layer (70) and the remaining metal layer (40) before patterning to form gate electrodes (90, 92) as shown in Fig. 1E and as described in paragraph [0029].

These are limitations set forth in claims 23, 28-30, 32-33 of the applicant's invention.

However, Rotondaro et al. do not expressly teach or suggest forming interconnects within dielectric layers located over the transistors to form an operational circuit, which are limitations of independent claim 23.

Referring to Fig. 4 and column 4, lines 33-61, Zhu et al. teach a method of forming a CMOS structure that includes forming inter level dielectric (ILD) (52) and inter metal dielectric (IMD) (55, 58) layers over field effect transistors (42, 44). The ILD and IMD layers include metal levels (54, 57, 59) that are interconnected using conductive vias (53, 56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Rotondaro et al. and Zhu et al. in order to include the formation of overlying dielectric layers with interconnections, as taught by Zhu et al. Zhu et al. recognize that a multi-level metallization network is used in integrated circuits for wiring discrete semiconductor devices (e.g. field effect transistors) together to thereby create desired circuits (see column 1, lines 14-19).

12. Claims 23, 25-27, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (US 6,890,807 B2) in view of Zhu et al. (US 6,133,079).

Referring to Figs. 3a-3d and column 5, line 6 to column 7, line 10, Chau et al. disclose a method of forming CMOS devices with metal gates that includes the following features:

- A metal layer (202) that can be molybdenum, tungsten, tantalum, or ruthenium (also see column 3, lines 9-28) is formed over a semiconductor substrate (200) (also see column 2, lines 17-30) as shown in Fig. 3a;
- Portions of the metal layer (202) corresponding to NMOS devices are masked with photoresist (216) (i.e. a protective layer) while the unmasked portions corresponding to PMOS devices are doped to increase the work function of the metal as shown in Fig. 3c;
- Dopants used to increase work function can include oxygen, which can be deposited using plasma deposition methods (also see column 4, lines 15-18, 34-38); and
- The metal layer (202) is then patterned to form gate electrodes (220, 230) corresponding to an NMOS device and to a PMOS device (220) as shown in Fig. 3d.

These are limitations set forth in claims 23, 25-27, 31 of the applicant's invention.

However, Chau et al. do not expressly teach or suggest forming interconnects within dielectric layers located over the transistors to form an operational circuit, which are limitations of independent claim 23.

Referring to Fig. 4 and column 4, lines 33-61, Zhu et al. teach a method of forming a CMOS structure that includes forming inter level dielectric (ILD) (52) and inter

metal dielectric (IMD) (55, 58) layers over field effect transistors (42, 44). The ILD and IMD layers include metal levels (54, 57, 59) that are interconnected using conductive vias (53, 56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Chau et al. and Zhu et al. in order to include the formation of overlying dielectric layers with interconnections, as taught by Zhu et al. Zhu et al. recognize that a multi-level metallization network is used in integrated circuits for wiring discrete semiconductor devices (e.g. field effect transistors) together to thereby create desired circuits (see column 1, lines 14-19).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ngo et al. teach the formation of silicon-rich tantalum silicon nitride by a plasma treatment that includes silane. Visokay et al. teach the formation of plural gate electrodes with different work functions. Cabral, Jr. et al. teach the formation of CMOS transistors featuring metal gate electrodes with different work functions.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot

STEPHEN W. SMOOT
PRIMARY EXAMINER